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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/006,610	12/03/2001	Jayson Trinh	01-53	1144

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EXAMINER	
GHULAMALI, QUTBUDDIN	
ART UNIT	PAPER NUMBER
2637	

DATE MAILED: 08/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/006,610	TRINH ET AL.	
	Examiner	Art Unit	
	Qutub Ghulamali	2637	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-23* is/are allowed.

6)☒ Claim(s) *24-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is responsive to the Amendment filed on 06/09/2005, in response to the office action of March 09, 2005.

Response to Arguments

2. Applicant's argument, filed 06/09/2005, with respect to claims 21, 31 and 34, has been considered, but is not persuasive.

The applicant's Remark/Argument of 06/09/2005, on pages 16-18, regarding claims 21, 31 and 34, have been fully considered but are not persuasive. The applicant indicates that Momtaz fail to teach the programmable feature for sync detect logic to assert a variable parallel clock enabling signal that controls the clock driver as recited in claim 24 and similarly recited in claims 31 and 34. On the contrary, Momtaz clearly shows in col. 9, lines 50-67 and col. 10, lines 1-25 the salient features comprise a microcontroller, digital signal processor operating under software or firmware program control such that parameters can be dynamically defined. Momtaz also clearly shows the pump-up and pump-down signal from the phase detector 42 or the phase and frequency detector 48 to the charge pump 52 in response to the logical state of the selection signal (col. 9, lines 35-45) which allows the median output frequency of the VCO to be established. A similar explanation is applied to claims 31 and 34. Therefore, in light of the above explanations, the examiner concludes that Momtaz discloses the limitations of the claimed

subject matter as anticipated. Accordingly, **THIS ACTION IS MADE FINAL**. The rejection under 35 USC 102(b) and 35 USC 103(a) is reiterated herein:

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) The invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 24, 30, 31, 34-37 are rejected under 35 U.S.C. 102(b) as being anticipated by Momtaz et al (US Patent 5,950,115).

Regarding claims 24 30, 31, 34-37, Momtaz discloses a deserializer comprising:

a clock divider (figs. 3, 4 elements 46, 66, 78) operable to receive a recovered clock signal (SCLK) and to generate a divided clock signal (RPCLK) for every given number of recovered clock signal cycles (col. 9, lines 20-34);

a serial-to-parallel shift register responsive to the recovered clock signal to shift in recovered serial data bits and responsive to the divided clock signal to shift out recovered parallel data bits (col. 7, lines 60-67; col. 8, lines 6-16); and

sync detect logic coupled to the clock divider and operable to assert a parallel clock enabling signal that enables the clock divider to generate the divided clock signal, the sync detect logic including a reloadable register operable to store a programmable synchronization bit pattern associated with a communications protocol and a bit pattern comparator operable to compare the stored programmable synchronization bit pattern with a synchronization bit pattern within the

recovered serial data bits and to assert or not assert the parallel clock enabling signal as a result of the comparison (col. 4, lines 4-14; col. 8, lines 20-51).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 25-29, 32, 33, are rejected under 35 U.S.C. 103(a) as being unpatentable over Momtaz et al (US Patent 5,950,115) in view of Anderson (US Patent 6,122,336) and further in view of Aung et al (US Pub. 2003/0212930).

Regarding claims 25 and 29, Momtaz discloses every feature of the claimed invention of claim 24 above. Momtaz, although discloses a phase detector (figs. 3, 4, elements 42, 74), does not explicitly disclose:

a phase detector operable to compare a serial data input (SDIN) with a recovered clock signal (SCLK) and to generate in response up and down signals;

a phase selector operable to select a clock signal as the recovered clock signal (SCLK) from a plurality of given clock signals in response to F'WD (forward) and BWD (backward) signals; and

a digital filter coupled between the phase detector and the phase selector, the digital filter operable to generate the FWD and BWD signals for the phase selector in response to the up and down signals received from the phase detector.

Anderson in the same field of endeavor discloses a Digital clock recovery circuit for generating a recovered clock signal comprising:

a phase detector (fig. 2, element 202) operable to compare a serial data input (SDIN) with a recovered clock signal (SCLK) and to generate in response up and down signals (col. 3, lines 9-13);

a phase selector (206) operable to select a clock signal as the recovered clock signal (SCLK) from a plurality of given clock signals (2N clock) in response to FWD (forward) and BWD (backward) signals (col. 3, lines 11-20); and

a digital filter (204) coupled between the phase detector (202) and the phase selector (206), the digital filter (204) operable to generate the FWD and BWD signals for the phase selector in response to the up and down signals (212, 214) received from the phase detector (202) (col. 3 lines 15-30). It would have been obvious to one skilled in the art at the time the invention was made to use a phase detector, a phase selector and a digital filter as taught by Anderson in the deserializer circuit of Momtaz so as to provide adequate detection and selection for an improved clock recovery.

Anderson, however, is silent regarding the specific details of the digital filter.

In the same field of endeavor, Aung discloses a clock data recovery circuit,

wherein the digital filter includes at least one reloadable register (multi stage shift register 200) (figs. 1-5) operable to store a programmable value for comparison (110; col. 3, section 0044) with a value derived from the up and down signals and a controller responsive to the comparison and operable to generate the FWD and BWD signals (col. 5, sections 0060, 0061). It would have been obvious to one skilled in the art at the time the invention was made to use shift registers to

store programmable values for comparison with a derived value from the up and down signals to generate signals as taught by Aung, in the clock recovery circuit of Anderson so as create perfect synchronism with the clock signal information embedded in the CDR.

Regarding claims 26 and 27, Momtaz, Anderson and Aung combined as a whole discloses every feature of the claimed invention 26 discussed above. Aung further discloses (fig. 4), a phase interpolator (162) coupled to a multiplexer (190) responsive to the FWD and BWD signals, the multiplexer operable to receive a plurality of given clock signals having different phases as inputs and to select each of at least two clock signals as one of the given clock signals as outputs, the phase interpolator operable to generate the recovered clock signal (SCLK) having a phase that is phase interpolated between the phases of the at least two selected clock signals (col. 4, sections 0052, 0053, 0054).

Regarding claim 28, Momtaz, disclose the DPLL is part of a data recovery circuit within a SERDES (serializer/deserializer) transceiver (abstract; fig. 2, col. 2, lines 1-7).

Regarding claims 32 and 33, Momtaz discloses every feature of the claimed invention of claim 31 above. Momtaz, however, does not explicitly disclose, multiplexer disposed after a plurality of bit comparators and select outputs of the bit comparators compare a respective synchronization bit pattern to said synchronization bit pattern within recovered serial data. Anderson is a similar field of endeavor discloses:

a multiplexer disposed before and after a plurality of bit comparators (figs. 8, 9 element 904) with said multiplexer selecting one of the outputs of the bit comparators as said parallel clock enabling signal depending on the communications protocol indicated by a MODE signal, and wherein each of said bit comparators compares a respective synchronization bit pattern to said

synchronization bit pattern within said recovered serial data bits (col. 4, lines 56-67; col. 5, lines 1-20.). It would have been obvious to one skilled in the art at the time the invention was made to use a multiplexer disposed after and before a plurality of bit comparators and select outputs of the bit comparators compare a respective synchronization bit pattern to said synchronization bit pattern within recovered serial data as taught by Anderson in the sync detect logic circuit of Momtaz because it can provide high phase resolution in recovered clock signals.

Allowable Subject Matter

7. Claims 1-23 allowed.

Reasons for Allowance

8. The following is an examiner's statement of reasons for allowance:

Regarding claims 1, 9 and 17, the prior of record does not teach or suggest in combination with other claim limitations a clock data recovery deserializer comprising:
a first bit pattern comparator that inputs an intermediate parallel data output (IPD0) from said serial-to-parallel shift register with each cycle of said recovered clock signal, wherein said serial-to-parallel shih register shifts in a bit of said recovered serial data bits every cycle of said recovered clock signal to generate said intermediate parallel data output (IPDO), and wherein said first bit pattern comparator compares for every cycle of said recovered clock signal said first predetermined number of bits of said intermediate parallel data output (IPDO) to said first synchronization bit pattern stored within said first reloadable register portion to assert a first comparator output signal when said first predetermined number of bits of said intermediate parallel data output (IPDO) is substantially same as said first synchronization bit pattern;

a second bit pattern comparator that inputs said intermediate parallel

data output (1PDO) from said serial-to-parallel shift register with each cycle of said recovered clock signal and that compares for every cycle of said recovered clock signal said second predetermined number of bits of said intermediate parallel data output (IPDO) to said second synchronization bit pattern stored within said second reloadable register portion to assert a second comparator output signal when said second predetermined number of bits of said intermediate parallel data output (IPDO) is substantially same as said second synchronization bit pattern.

Such limitations as recited in claims 1, 9 and 17 above, are neither anticipated nor rendered obvious by the prior art of record.

Claims 2-8, 10-16 and 18-23 are allowed by virtue of their dependency to claims highlighted above.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Qutub Ghulamali whose telephone number is (571) 272-3014. The examiner can normally be reached on Monday-Friday from 8:00AM - 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on (571) 272-2988. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

QG.
August 19, 2005.

JAY K. PATEL
SUPERVISORY PATENT EXAMINER